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RENESAS TECHNICAL UPDATE

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Product Category	MPU&MCU		Document No.	TN-SH7-A639A/E	Rev.	1.00
Title	SH7780 Mask-changed Product Specification for revised DDRIF and PCIC		Information Category	Technical Notification		
Applicable Product	SH7780 (R8A77800A, R8A77800B)	Lot No. All lots	Reference Document	SH7780 Hardware Manual Rev.1.00 Dec. 13, 2005 (REJ09B0158-0100)		

This information summarizes the SH7780 spec explaining the differences between the current product and the mask-changed product for revised DDRIF and PCIC.

Note that, only the DDRIF and PCIC limitations that described below have been fixed in this mask-changed product, and other limitations of the SH7780 are not fixed and same with the R8A77800A.

Refer also to the technical updates of the R8A77800A except in case there is a special notification.

The current product (R8A77800A) that has the DDRIF and PCIC limitations will be discontinued.

Please change to the mask-changed product as soon as possible whether or not applied this limitation.

[Specification comparison of current R8A77800A vs. mask-changed R8A77800B]

1. Limitation of DDR-SDRAM bus operating frequency of DDRIF

a) Current product (R8A77800A)

When using clock mode 0, 1, 2 or 3 of the SH7780, the DDR-SDRAM bus operating frequency (MCLK frequency) is 134 MHz or more, according to the operating condition of the LSI, the internal VDD and ground are influenced, and the access from the DDRIF to the DDR-SDRAM may not be performed correctly.

b) Mask-changed product (R8A77800B)

The limitation of the DDR-SDRAM bus operating frequency is fixed and the access from the DDRIF to the DDR-SDRAM is performed correctly even in clock mode 0, 1, 2 or 3 (MCLK frequency is 134 MHz or more).

2. VDD/VDD-PLL/VDD-DLL power supply voltage

The maximum voltage of VDD, VDD-PLL1/2/3 and VDD-DLL1/2 are as follows.

(Gray parts are different)

Item	Symbol	Current Product (R8A77800A) (When using DDRIF, only clock mode 12 is available (MCLK frequency is up to 134 MHz))					Mask-changed Product（R8A77800B）				
		Min.	Typ.	Max.	Unit	Test Condition	Min.	Typ.	Max.	Unit	Test Condition
Power supply voltage	VDD VDD-PLL 1/2/3 VDD-DLL 1/2	1.15	1.25	1.35	V	Normal operation (DDR266), sleep mode	1.15	1.25	1.365	V	Normal operation (DDR320/266), sleep mode

3. Limitation of PCIC

a) Current product (R8A77800A)

When using the PCIC with the following condition, the PCIC target read data may be lost.

Note that, there is no problem about the target write access.

Even though following conditions exist, the internal SuperHyway bus clock frequency (SHck) is higher than the frequency of the PCI clock (PCICLK) multiplied by 3.3, and the target read transaction between the PCIC and the DDR-SDRAM, the read data is never lost. (For example, when SHck is 133.0MHz, PCICLK must be lower than 40.3MHz)

[Condition]

The following three conditions exist at the same time.

- PCICR.PFCS=1 (32-byte pre-fetching)
- PCICR.FTO=1 (TRDY# control enable)
- PCICR.PFE=1 (Pre-fetch enable)

[Workaround]

Take 1 or 2 workaround when using the PCIC with above condition.

1. Use always the master operation.
2. Use the PCIC excluding at least one of the terms and conditions above.

b) Mask-changed product (R8A77800B)

The limitation of the PCICR settings, the relationship of the operating frequency between the SuperHyway bus (SHck) and the PCI bus (PCICLK) and the limitation of the transfer section are fixed. The target read data is not lost.

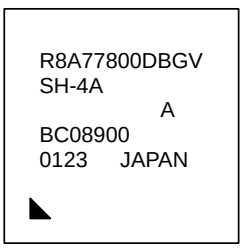
4. Product register value

Register name	Abbrev.	Current Product（R8A77800A）	Mask-changed Product (R8A77800B)
Product register	PRR	H'0000092x	H'0000093x

5. Part number of mask-changed products

Product Name	Part Number		Operating Temperature	Package
	Current Product	Mask-changed Product		
SH7780	R8A77800ANBG	R8A77800BNBG	-20 to +75 °C	449-pin BGA
	R8A77800ANBGV	R8A77800BNBGV		449-pin BGA (lead-free)
	R8A77800ADBG	R8A77800BDBG	-40 to +85 °C	449-pin BGA
	R8A77800ADBGV	R8A77800BDBGV		449-pin BGA (lead-free)

6. Mark example

Current Product (R8A77800A)		Mask-changed Product (R8A77800B)	
Leaded	Lead-Free	Leaded	Lead-Free
			

Note. Marking line 3 identifies mask code (B: mask-changed product).

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